

This listing of claims replaces all prior listings of the claims in the application.

In the Claims:

1. (currently amended) An integrated circuit having complementary metal oxide semiconductor (CMOS) transistors including a p-type field effect transistor (PFET) and an n-type field effect transistor (NFET), said PFET and said NFET each having a channel region and source and drain regions disposed in a first semiconductor region having a first composition, wherein a first strain is applied to ~~the~~ said channel region of ~~the~~ said PFET but not to said channel region of the said NFET via ~~a~~ a second semiconductor layer regions having a second composition lattice-mismatched to said first semiconductor region, said second semiconductor regions underlying said ~~disposed in~~ source and drain regions of ~~the~~ said PFET, ~~and but not underlying said channel region of said PFET and not underlying said~~ of the NFET, ~~said semiconductor layer being lattice-mismatched to a single crystal semiconductor disposed in said channel regions of said PFET and said NFET.~~

2. (cancelled)

3. (currently amended) The integrated circuit of claim 2-1 wherein said ~~single crystal region of said~~ first semiconductor region has a main surface defined by a level of a gate dielectric of a gate stack of said PFET and ~~said layer of said second semiconductor regions have~~ has a top surfaces disposed beneath said main surface.

4. (cancelled)

5. (currently amended) The integrated circuit of claim 1 wherein said first composition of said first semiconductor region is ~~consists essentially of a semiconductor~~ selected from the group consisting of silicon, silicon germanium and silicon carbide and said second composition of said second semiconductor regions is ~~consists essentially of~~ another composition semiconductor ~~different from said first composition semiconductor~~, said another ~~semiconductor composition~~ selected from the group consisting of silicon, silicon germanium and silicon carbide.

6. (currently amended) The integrated circuit of claim 1 wherein said first ~~semiconductor composition~~ consists essentially of silicon and said second ~~semiconductor composition~~ consists essentially of silicon germanium.

7. (currently amended) The integrated circuit of claim 1 wherein said first ~~semiconductor composition~~ consists essentially of silicon germanium according to a first formula  $\text{Si}_{x1}\text{Ge}_{y1}$ , where  $x1$  and  $y1$  are percentages,  $x1 + y1 = 100\%$ ,  $y1$  being at least one percent and said second ~~semiconductor composition~~ consists essentially of silicon germanium according to a second formula  $\text{Si}_{x2}\text{Ge}_{y2}$ , where  $x2$  and  $y2$  are percentages,  $x2 + y2 = 100\%$ ,  $y2$  being at least one percent, wherein  $x1$  is not equal to  $x2$  and  $y1$  is not equal to  $y2$ .

8. (original) The integrated circuit of claim 1 wherein said first strain is a

compressive strain.

9. (currently amended) The integrated circuit of claim 6 wherein said second ~~semiconductor~~ composition consists essentially of silicon germanium having a germanium content of at least one percent.

10. (currently amended) The integrated circuit of ~~claim 4~~ claim 1, further comprising wherein each of said PFET and said NFET further comprise a layer of silicide regions contacting gate conductors, and said source regions and said drain regions of said PFET and said NFET.

11. (currently amended) The integrated circuit of claim 10 wherein said silicide regions ~~consists~~ consist essentially of a silicide of cobalt.

12. (currently amended) An integrated circuit having complementary metal oxide semiconductor (CMOS) transistors including a p-type field effect transistor (PFET) and an n-type field effect transistor (NFET), each the NFET and the PFET each having a channel regions-region and source and drain regions disposed in a first semiconductor region consisting essentially of silicon, single-crystal silicon regions of a substrate wherein a first strain is applied to the channel region of the PFET but not to the channel region of the NFET via a via buried lattice-mismatched semiconductor layer regions consisting essentially of silicon germanium disposed in underlying the source and drain regions of the PFET but not underlying the channel region of the PFET and

not underlying of the NFET, said silicon germanium of said buried lattice-mismatched semiconductor regions having ~~proportions~~ a composition according to the formula  $\text{Si}_x\text{Ge}_y$  where x and y are percentages each being at least one percent, x plus y equaling 100 percent.

13. (withdrawn) A method of fabricating a p-type field effect transistor (PFET) and an n-type field effect transistor (NFET), said NFET and said PFET each having a channel region, said channel region of said PFET having a first strain and said channel region of said NFET not having said first strain, said method comprising:

forming a PFET gate stack and an NFET gate stack over a main surface of a single-crystal region of a first semiconductor, each of said PFET gate stack and said NFET gate stack including a gate dielectric, a gate conductor formed thereon, a cap layer formed over said gate conductor and first spacers formed on sidewalls of said gate conductor;

recessing said single-crystal region on sides of said PFET gate stack while protecting said main surface of said single-crystal region on sides of said NFET gate stack from being recessed;

growing a layer of a second semiconductor in areas of said single-crystal region exposed by said recessing while preventing said layer from growing on said single-crystal region on sides of said NFET gate stack, said second semiconductor being lattice-mismatched to said first semiconductor to apply said first strain to said channel region of said PFET; and

fabricating source and drain regions on said sides of said PFET gate stack

to form said PFET and fabricating source and drain regions on said sides of said NFET gate stack to form said NFET.

14. (withdrawn) The method of claim 13 further comprising recessing said layer of second semiconductor below said main surface of said single-crystal region.

15. (withdrawn) The method of claim 14 further comprising growing a layer of said first semiconductor over said recessed second semiconductor layer.

16. (withdrawn) The method of claim 15 further comprising forming a self-aligned silicide (salicide) over said source and drain regions of said PFET and of said NFET.

17. (withdrawn) The method of claim 16 further comprising forming a self-aligned silicide (salicide) over polysilicon portions of said gate conductors of said PFET and said NFET.

18. (withdrawn) The method of claim 17 wherein said silicide includes a silicide of cobalt.

19. (withdrawn) The method of claim 15 wherein said first semiconductor comprises silicon and said second semiconductor comprises silicon germanium, said silicon germanium having a germanium content of at least one percent.

20. (withdrawn) The method of claim 19 wherein said lattice-mismatched second semiconductor applies a compressive strain to said channel region of said PFET.

21. (withdrawn) The method of claim 13 wherein said step of forming said source regions and drain regions further includes removing said first spacers from said PFET gate stack and said NFET gate stack and forming second spacers on sidewalls of said PFET gate stack and said NFET gate stack.

22. (withdrawn) The method of claim 21 wherein said second spacers have a greater thickness than said first spacers.

23. (withdrawn) The method of claim 21 further comprising halo implanting exposed areas of said single-crystal region and said layer of said first semiconductor.

24. (withdrawn) The method of claim 21 further comprising extension implanting exposed areas of said single-crystal region and said layer of said first semiconductor.

25. (withdrawn) The method of claim 22 further comprising forming third spacers laterally contacting said second spacers, and implanting source and drain regions in said exposed areas of said single-crystal region and said layer of said first

semiconductor.

26. (withdrawn) The method of claim 13 wherein said single-crystal region on said sides of said NFET gate stack are prevented from being recessed by a patterned block mask.

27. (withdrawn) The method of claim 13 wherein said second semiconductor layer is prevented from growing on said single-crystal region on said sides of said NFET gate stack by applying a first coating to said single-crystal region on said sides of said NFET gate stack.

28. The method of claim 27 wherein said coating is formed conformally over an exposed surface of said single-crystal region including over said PFET gate stack and said NFET gate stack.

29. (withdrawn) The method of claim 28 further comprising stopping said recessing of said single-crystal region on said sides of said PFET stack and forming a second coating on said areas of said single-crystal region exposed by said recessing, and thereafter continuing said recessing, such that said second semiconductor does not grow in areas protected by said second coating.

30. (withdrawn) The method of claim 29 further comprising growing a layer of said first semiconductor on said layer of said second semiconductor.

31. (withdrawn) The method of claim 30 wherein said first semiconductor comprises silicon and said second semiconductor comprises silicon germanium, said silicon germanium having a germanium content of at least one percent.

32. (withdrawn) The method of claim 29 wherein said second semiconductor applies said first strain as a compressive strain.

33. (new) The integrated circuit of claim 1 wherein the second semiconductor regions are thin epitaxial layers disposed in trenches adjacent to said channel region of said NFET.